AMENDMENT

In The Claims:

Please amend the claims as follows:

Claim 1. (Currently amended) An electrostatic discharge (ESD) protection circuit, comprising:

a silicon controlled rectifier (SCR) circuit, which comprises a first connection terminal, a second connection terminal, and a third connection terminal, wherein the first connection terminal and the second connection terminal are respectively and directly connected to an I/O pad and a ground voltage, so as to discharge the electrostatic charges;

an anti-latch-up circuit, which comprises a fourth connection terminal directly connected to a voltage source, a fifth connection terminal directly coupled to the ground voltage, and a sixth connection terminal directly connected to the third connection terminal of the SCR circuit; and

a first diode, having ~~a first input end coupled~~ an anode directly connected to the I/O pad and a ~~second input end coupled~~ cathode directly connected to the fourth connection terminal, wherein when an over positive voltage does not occur on the I/O pad, the first diode is not conducted, and the anti-latch-up circuit substantially generates an anti-latch-up signal to the third connection terminal of the SCR circuit according to the voltage source so as to prevent latching up of the SCR circuit during normal operation, and when the over positive voltage occurs on the I/O pad, the first diode is conducted, and the anti-latch-up circuit does not substantially generate the anti-latch-up signal in response to the conduction of the first diode.

Claim 2. (Previously Presented) The ESD protection circuit of claim 1, further comprising:

a second diode, having a first input end and a second input end, respectively connected to the ground voltage and the I/O pad.

Claim 3. (Previously Presented) The ESD protection circuit of claim 1, wherein the SCR circuit comprises:

a P-type substrate;

an N well, formed in the p-type substrate;

a first P+ doped region, formed in the P-type substrate and coupled to the ground voltage;

a first N+ doped region, formed in the P-type substrate, adjacent to the first P+ doped region, and coupled to the ground voltage;

a second N+ doped region, formed between the P-type substrate and the N well, adjacent to the first N+ doped region, coupled via the third connection terminal of SCR circuit to the sixth connection terminal of the anti-latch-up circuit, serving as a guard ring to collect electrons to avoid latch up when the anti-latch-up circuit sends the anti-latch-up signal through the sixth connection terminal to the third connection terminal of the SCR circuit during normal operation, and floating when the anti-latch-up circuit sends no signal to the SCR circuit during an ESD event;

a second P+ doped region, formed in the N well, adjacent to the second N+ doped region, and coupled to the I/O pad; and

a third N+ doped region, formed in the N well, adjacent to the second P+ doped region, and coupled to the voltage source;

wherein a diode is coupled to the second P+ doped region and the I/O pad at one end and coupled to the other end.

Claim 4. (Original) The ESD protection circuit of claim 3, wherein the anti-latch-up circuit comprises:

a capacitor, having a first contact end and a second contact end, respectively coupled to the second N+ doped region and the ground voltage; and

a resistor, having a first end and a second end, respectively coupled to the voltage source and the second N+ doped region.

Claims 5 – 12 (Canceled)

Claim 13. (Previously Presented) The ESD protection circuit of claim 1, wherein the anti-latch-up signal sent from the sixth connection terminal to the SCR circuit comprises a voltage signal.

Claim 14. (Canceled)

Claim 15. (Previously Presented) The ESD protection circuit of claim 1, wherein a RC delay time of the anti-latch-up circuit is smaller than a voltage rising time of an IC power but greater than a voltage rising time of an ESD pulse.